The Examiner's Action mailed on Oct. 3, 2001 has been received and its contents carefully considered.

In this Amendment, Applicants have editorially amended the specification, and Figures 1 through 8, and added claims 23 through 29. Moreover, claims 13 through 19 have been canceled. Claims 1 through 12, and 20 through 29 are pending in the application. Claims 1, 20 and 23 are the independent claims. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner has objected to the drawings for not properly crosshatching the Figures. In response thereto, submitted for the Examiner's approval are proposed drawing changes, with the changes indicated in red ink. In particular, the dielectric layer and the insulating layers have been shown with crosshatching. Upon approval of the drawing changes and allowance of the application, revised formal drawings will be submitted in compliance with United States Patent and Trademark Office guidelines. The revised formal drawings will include crosshatching of the insulating and dielectric layers that is in compliance with official guidelines. It is requested that this objection be withdrawn.

The Examiner has further objected to the drawings for not illustrating the conductive pad being electrically coupled to the signal trace, such as recited within claim 20. However, the Examiner's attention is respectfully directed to Figure 9, where this feature is clearly shown. It is thus requested that this objection be withdrawn.

The Examiner has objected to the disclosure for an informality. In response thereto, the specification has been editorially corrected to correct the informality specifically noted by the Examiner. It is requested that this objection be withdrawn.

The Examiner has rejected claims 1 through 3, 5 through 12 and 20 through 21 has been indefinite. In particular, the Examiner states claim 1 is incomplete for ommitting essential structural cooperative relationships. In particular, the Examiner queries how the conductive pad can be located on the dielectric layer and in the hole at the same time.

It is initially noted that claim 1 does not recite this alleged relationship. Instead, claim 1 simply recites that the conductive pad has a majority thereof within an area defined by an outer periphery of the hole. There is no recitation within claim 1 that the conductive pad is located on the dielectric layer, as alleged by the Examiner's Action. Moreover, there is no recitation from claim 1 that the conductive pad is located in the hole, as alleged by the Examiner's Action. As such, is submitted that Applicants' independent claim 1 complies with all official provisions, and it is requested that this rejection be withdrawn.

The Examiner has further rejected claims 6 and 20 for using the term "majority". The Examiner queries what is a majority. However, the Examiner's attention is respectfully directed to page 11, lines 2 through 5, where this term is defined as meaning over 50 percent. Moreover, one skilled in the art would know that this is the common usage of this term. Since this term is clearly and fully defined by Applicants' specification and is used in the claims in the manner commonly associated with this term, it is submitted that claims 6 and 20 are definite within the purview of 35 USC Section 112, second paragraph, and it is requested that this rejection be withdrawn.

The Examiner has rejected claims 1 through 3, 6 through 11 and 20 and 21 has been anticipated by *Ohshima et al.* (USP 5,455,393). It is submitted that these claims are patentably distinguishable over the cited reference for at least the following reasons.

It is well settled that a reference may anticipate a claim within the purview of 35 USC Section 102 only if all the features and all the relationships recited in the claim are taught by the reference structure either by clear disclosure or under the principal of inherency.

Applicants' independent claim 1 is directed to a surface laminar circuit board. The circuit board includes an insulating layer, and a conductive layer on the insulating layer. The conductive layer has a hole formed therein.

A conductive pad is provided that has a majority thereof within an area defined by an outer periphery of the hole. These claimed features are not disclosed by the cited reference.

The cited reference is directed to a multilayered printed wiring board. This reference discloses forming first parallel grooves 104 within a photosensitive resin (insulating layer) 103. A first plated copper 105 is deposited within the first grooves 104. The plated copper is not deposited on portions except for the first grooves 104 (see column 4, lines 49 and 50, and lines 61 through 65). This reference further discloses forming circuits 106 between the respective first grooves 104. This reference discloses that the circuits 106 have a wiring pattern that parallels the first grooves 104 (see column 5, lines 21 through 23).

This reference additionally discloses forming a second insulating layer 108 over the circuits 106. Moreover, this reference discloses forming a second ground layer 110

over the second insulating layer 108, and forming parts mounting pads 112 over and direct contact with the second ground layer 110 (see Fig. 1 G).

The Examiner's Action has equated the insulating layer 103 as being equivalent to Applicants' claimed insulating layer. The Examiner's Action has further equated the conductive circuits 106 as being the equivalent of Applicants' claimed conductive layer. The Examiner's Action has further equated the second insulating layer 108 as being the equivalent of Applicants' claimed dielectric layer. Moreover, the Examiner's Action has equated the parts mounting pads 112 as being the equivalent of Applicants' claimed conductive pad.

The Examiner's Action states that the spaces between the reference number 103 constitute a hole within a conductive layer 106. However, it is initially noted that this reference discloses that these spaces are parallel grooves formed within the layer 103, and that the circuits 106 are disposed parallel to and between these grooves. It is unclear how the Examiner's Action can possibly consider these parallel grooves as being a hole formed within the circuits 106 which would be the interpretation required to render Applicants' claimed invention anticipated. Moreover, there's no disclosure from this reference that any of the circuits 106 have a hole formed therein, such as would be required to render Applicants' claimed invention anticipated. Further, although the circuits 106 are arranged parallel to and spaced apart from each other, the space between the individual circuits 106 does not constitute a hole formed in a circuit.

Moreover, Applicants' claimed invention recites that the conductive pad has a majority thereof within an area defined by an outer periphery of the hole. Even assuming that the parallel grooves formed within the insulating layer 103, or the spaces

between adjacent ones of the circuits 106, could be construed in some manner as being a hole, the conductive pads 112 are not formed with a majority thereof within an area defined by an outer periphery of such "holes". As such, it is submitted that Applicants' independent claim 1 has not been anticipated by the cited reference.

Furthermore, Applicants' dependent claims 2, 3, and 6 through 11 are submitted to be patentably distinguishable over the cited reference for at least the same reasons as independent claim 1, from which these claims respectively depend, as well as for the additional features recited therein. Moreover, Applicants' dependent claim 3 is submitted to be further patentably distinguishable over the cited reference in that this claim recites that the conductive pad is disposed directly on an upper surface of the photosensitive dielectric layer. However, it is noted that the pad 112 disclosed by the cited reference is separated from the insulating layer 108 (which the Examiner's Action has equated to being the equivalent of Applicants' claimed dielectric layer) by the second ground layer 110. Thus, the pad 112 is disposed directly upon the second ground layer 110 rather than directly upon the insulating layer 108 as would be required by Applicants' claim 3.

Moreover, Applicants' dependent claim 6 is submitted to be further patentably distinguishable over the cited reference in that this claim recites that the conductive layer comprises a signal ground layer. The Examiner's Action contends that this feature is disclosed by the cited reference. However, the cited reference makes clear that the feature 106, which the Examiner has equated to being the equivalent of Applicants' claimed conductive layer, is a circuit, whereas the features 102 and 110 are the ground

layers. However, these ground layers do not meet the requirements of Applicants' claimed conductive layer.

Furthermore, Applicants' dependent claims 9 and 10 are submitted to be further patentably distinguishable over the cited reference in claim 9 recites that the photosensitive dielectric layer has a thickness in a region over the conductive layer, that is less than about 50 micrometers. Claim 10 recites that the thickness of the dielectric layer in this region is equal to or less than about 40 micrometers. The Examiner refers to column 4, line 60 of the cited reference as evidence that this feature is disclosed by the cited patent. However, this portion of the patent is referring to the thickness of the first insulating layer 103, which the Examiner's Action has previously equated as being the equivalent of Applicants' claimed insulating layer, rather than to the thickness of the insulating layer 108, which the Examiner's Action has previously equated as being the equivalent of Applicants' claimed dielectric layer. Moreover, there is no disclosure from this reference of the thickness of the insulating layer 108, much less the thickness of the insulating layer 108 in a region over the circuits 106, such as would be required by Applicants' claims 9 and 10.

Applicants' independent claim 20 recites features similar to those discussed above with respect to claims 1 through 3 and 6 through 11. It is submitted that this claim is patentably distinguishable over the cited reference for at least the following reasons.

Applicants' independent claim 20 recites a surface laminar circuit board that includes, *inter alia*, a signal ground conductive layer disposed on an upper surface of the insulating layer. The conductive layer has a hole formed therein.

It is noted that the Examiner's Action refers to reference number 103 as being a conductive layer; however, this feature 103 is an insulating layer. It is thus presumed that the Examiner's Action intended to rely upon the circuits 106 in this regard, similar to the rejection presented against claim 1.

However, as previously argued, the circuits 106 are not signal ground layers. Instead, this reference discloses that the layers 102 and 110 are the ground layers. Moreover, and as previously argued, none of the circuits 106 have a hole formed therein. Instead, this reference discloses arranging the circuits 106 in a parallel pattern so that the individual circuits 106 are disposed between, and parallel to, the parallel grooves 104.

Furthermore, Applicants' claimed invention recites that a signal trace is disposed on the photosensitive dielectric layer and is electrically coupled with the signal ground conductive layer by way of a photo micro-via. The Examiner's Action has equated the claimed photo micro-via as being met by the copper 109 that is disposed within the grooves 107. However, this reference discloses that it is the first and second ground layers 102, 110 that are electrically coupled together utilizing the plated copper 109. There is no disclosure from this reference that the circuits 106 (which the Examiner has equated to being a signal ground conductive layer) are electrically coupled to the ground layer 110 (which the Examiner has equated to being a signal trace) using plated copper 109 (which the Examiner has equated to being a photo micro-via), as would be required by Applicants' independent claim 20.

Furthermore, and as argued above, the cited reference does not disclose a conductive pad having a majority thereof within an area defined by an outer periphery of

the hole. As such, it is submitted that Applicants' independent claim 20 has not been anticipated by the cited reference.

Applicants' dependent claim 21 is submitted to be patentably distinguishable over the cited reference for at least the same reasons as independent claim 20, from which this claim depends. Moreover, claim 21 is submitted to be further patentably distinguishable over the cited reference in that this claim recites that the conductive pad is disposed directly on an upper surface of the photosensitive dielectric layer. As discussed above, the cited reference does not disclose this feature. As such, it is submitted that the claims have not been anticipated by the cited reference, and it is requested that these rejections be withdrawn.

The Examiner has rejected claims 5, 12 and 20 as being obvious over *Ohshima et al.* Because the Examiner's Action does not address the rejection of claim 20 within this portion of the Action, and because the Examiner's Action did reject claim 20 as being anticipated by this same reference, Applicants have presumed that this was a typographical error, and that the rejection should have been addressed only to the claims 5 and 12. Applicants will thus respond to this rejection accordingly.

As noted above, Applicants' independent claim 1 is patentably distinguishable over the cited reference. As such, dependent claims 5 and 12 are patentably distinguishable over the cited reference for at least the same reasons as independent claim 1, from which these claims depend. Moreover, claim 12 is submitted to be further patentably distinguishable over the cited reference in that this claim recites that the conductive pad is disposed completely within the area defined by the outer periphery of the hole. As disclosed by Applicants' specification, this is a preferred aspect of the

invention (see page 11, lines three through five). This configuration eliminates the cause of the high parasitic capacitance that is found in the conventional surface laminar circuit boards, and increases the area through which the dielectric layer can be bonded to the underlying insulating layer, thereby increasing the bonding strength of the dielectric layer and reducing the risk of the delamination of the surface laminar circuit board, especially in a region of the pads (see page 13, lines 8 through 16).

The Examiner's Action states that this feature would be an obvious matter of design choice. However, in view of the fact that Applicants' specification discloses advantageous reasons for this configuration, as discussed above, it is submitted that the Examiner's Action has failed to establish a *prima facie* case of obviousness against this claim. It is thus requested that these claims be allowed and that these rejections be withdrawn.

It is submitted that this application is in condition for allowance. Such action, and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

December 28, 2001
Date

Robert H. Berdo, Jr.
Registration No. 38,075
Customer No. 23995
(202) 659-1915
(202) 659-1898 (facsimile)

RHB:crh

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Page 13, lines 5-7, please replace the paragraph thereon with the following replacement paragraph:

--Figure 9 is a top-down view of an exemplary aspect of the invention, illustrating the positioning of the pads [16] 22. As shown, the hole 16 has a rectangular shape. However, the hole 16 may have other shapes without departing from the invention.--